**North SouthUniversity**

Department of Computer Science and Engineering

Quiz-6, Section – 5, Spring-2017

Course No: **CSE 231** Course Title: **Digital Logic Design**

Time:20 min Full Marks: 10

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| 1. | Design a 6 bit Johnson Counter | 3 |
| 2. | Reduce the number of state in the following state table, tabulate the reducedtable, and draw the state diagram   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Present State** | **Next State** | | **Output** | | | **x = 0** | **x = 1** | **x = 0** | **x = 1** | | *a* | *f* | *b* | 0 | 0 | | *b* | *d* | *c* | 0 | 0 | | *c* | *f* | *e* | 0 | 0 | | *d* | *g* | *a* | 1 | 0 | | *e* | *d* | *c* | 0 | 0 | | *f* | *f* | *b* | 1 | 1 | | *g* | *g* | *h* | 0 | 1 | | *h* | *g* | *a* | 1 | 0 | | 7 |